

## Design and Performance Analysis of Programmable Digital Delay Generator

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**Abstract:** Delays are used in a variety of ways in Nuclear and High Energy Physics experiments which often deal with a large number of detectors. These detectors give out analog signals depicting several parameters like pulse height, width, time of arrival, pulse count rate etc. Some or all of these analog signals have to be used to validate the event as well as to extract its parameters before recording; some of these signals are to be delayed to participate in the final trigger generation. Usually, for digital delay, TTL / ECL / Delay ICs based delay modules are used to provide required delay for these signals, so that the active participation of these signals can be judged / determined. We have designed and developed an FPGA based programmable digital delay module. This module can be used using a CAMAC standard for programmability. We discuss the design aspects as well as the performance of a proto-type module in this paper.

**Keywords:** Cyclone IV, CAMAC, ECL, FPGA, Masking, NIM, Remotely Controlled, LVTTTL.

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### I. Introduction

Nuclear and High Energy Physics experiments<sup>[1] [2]</sup> often deal with a large number of information channels derived from detectors which constitute the information of an event of interest. Many detectors produce analog signals with many information like pulse height, width, time of arrival, pulse count rate etc. Some or all of these analog signals have to be used to validate the event as well as to extract its parameters before recording.

Usually, all these signals crossing a set threshold are converted to digital form using a fast discriminator<sup>[3] [4]</sup>. After digital conversion, these signals are to be delayed by different delay values to make them useful to participate in a valid event as well as to find out the timing information for a particular detector / sensor output, and to bring them within a specified trigger window etc<sup>[5] [6]</sup>.

Delays are necessary in the following manners in these experiments.

- Different delays are required to observe the sources at different zenith angles.
- To delay a signal with respect to a common event, this will be used to find out the direction information.
- To compensate the delay, introduced by the electronic modules, cables which are used for intermediate connections in the Data Acquisition System.
- To delay a signal so that it can be brought within the specified window, that is framed for data recording purpose.

There are many ways by which a fixed amount of delay can be introduced.

- Coaxial cable (for example RG 58 provides an approximate delay of 5ns / meter with 50  $\Omega$  impedance)<sup>[7]</sup>.
- Monostable Multivibrators (Monoshots) using Transistor Transistor Logic (TTL) / Emitter Coupled Logic (ECL) / Integrated Circuits (ICs)<sup>[8] [9]</sup>.
- Digitally Programmable Delay Generator ICs<sup>[9]</sup>.
- Different delay ICs<sup>[10]</sup>.

Many commercial delay generator modules are available with manual or programmable adjustment. The delay of these module are changed online or offline as per the need of experiment.

Many times it is essential to adjust and control the delay of each channel individually or to set different delays for different groups of detector outputs as per the need of the analysis of data or depending upon the observation one is interested, as done, for example, in experiments searching for sources of high energy celestial  $\gamma$ -rays using atmospheric Cherenkov radiation<sup>[1] [2]</sup>. The Cherenkov light pool produced by primary  $\gamma$ -rays or cosmic-rays in the atmosphere lasts for a few nanoseconds (ns). It is sampled during moon less dark nights by an array of Atmospheric Cherenkov telescopes in these ground-based experiments. Photomultiplier tubes (PMT) mounted at the focus of the light collector converts the light to electrical signal. The shape of the PMT pulse depends on the density and the arrival time distribution of Cherenkov photons and on the response of the detector elements. Due to large area of collection, there is a spread in the arrival time of photons, which causes

fluctuations in the shape and arrival time of the pulse. Experimentally, it is observed that the shape and arrival time of individual pulses varies from event to event. These experiments have hundreds of fast analog channels of information which have to be delayed using delay module for fast trigger (event) validation, data recording as well as for monitoring purpose<sup>[3] [4]</sup>.

The delay of each mirror-PMT system has to be maintained uniformly throughout the observation. This could be achieved by using delay generator module with programmable delay and width. Thus there was a need for independent and remote adjustment of several delays. Keeping this experiment in mind, we have designed and simulated a general purpose FPGA based programmable delay generator module for using in the CAMAC<sup>[11]</sup> standard of data acquisition system<sup>[4]</sup>.

Our design of FPGA based Programmable delay generator<sup>[12]</sup> module has independent programmable delay as well as width adjustment. It is designed on a CAMAC standard for programmability. We discuss here the design features of this module including the circuit diagram and the simulation results along with the performance. The digital delay architecture has been designed in VHDL with an Altera Cyclone FPGA (EP1C20F400C8)<sup>[13]</sup> as a target device, Simulations are done with FPGA (EP4CE115F29C7) on Altera DE2-115 Evaluation Board, Altera Quartus II version 11.0, and ModelSim Altera starter edition 10.0 C<sup>[13] [14]</sup>.

## II. Basic principle of Delay Generator

Analog pulses of varying amplitude and shape are generated randomly in time by the detectors or transducers used in high energy experiments. The discriminators are generally used to convert these analog pulses to more practical digital world. At the output it produces a standard pulse which is related in time to the leading edge crossing of the threshold<sup>[4]</sup>. The output pulse has a constant height and width, which is completely independent of all other characteristics of the input signal, except for its time of arrival. After the digitization of these analog signals, these signals have to be delayed by a certain amount to make them useful in event participation, to calculate the timing information, to use them as trigger input, monitoring purpose etc.

In general, these delay generator / module are designed as shown in Fig. 1. In these designs, in one method, the required delay is produced by a combination of two retriggerable monostable multivibrators (monoshot) which are operating in non-retriggerable mode, and the pulse width of each monoshot is controlled by a combination of external timing components resistance (R) and capacitance (C). In most of the cases C is fixed and the value of R is varied by a potentiometer, which sets a current which is linear discharge rate of the capacitor, to get a desired pulse width.

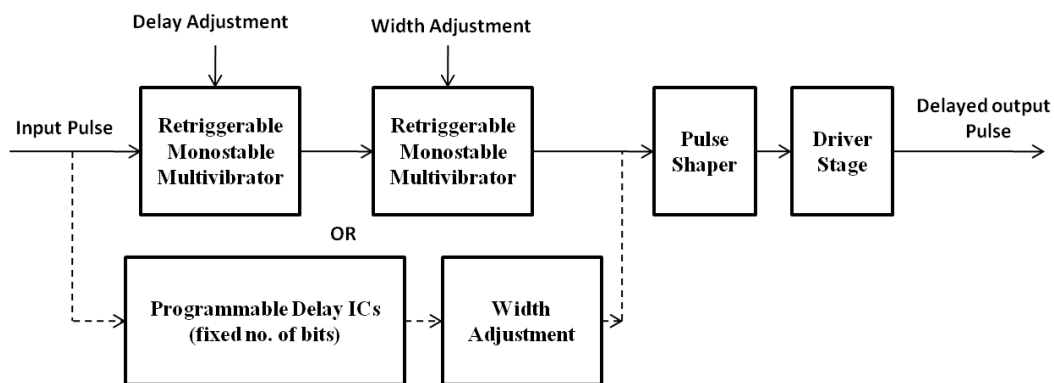
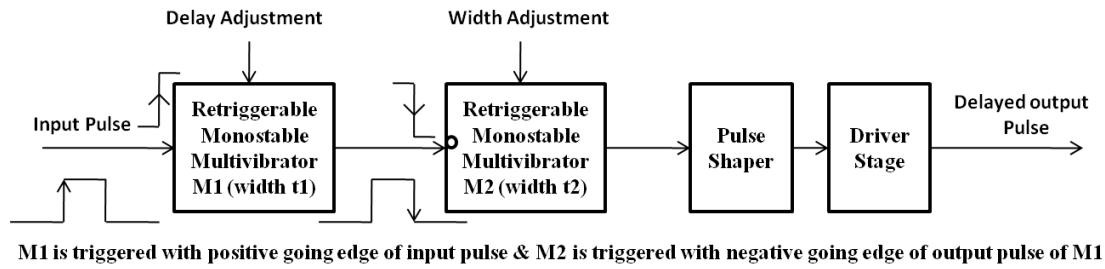


Figure 1: Basic block diagram of Delay Generator

Each monoshot can be triggered by any combination of positive or negative edges. By adjusting the different pulse widths for both the monoshots, one can get desired delay and pulse width of the output signal w.r.t. the input pulse. If the pulse width adjusted for first monoshot is  $t_1$  and for second monoshot is  $t_2$  respectively and then if the first monoshot is triggered by the positive edge of the input pulse and the second monoshot is triggered by the negative edge of the non inverted output pulse (Q) of the first monoshot, as represented in the Fig. 2, then the output pulse will be a delayed pulse with a delay of  $(t_1 + t_{pd1} + t_{pd2})$  time and will be having a width of  $t_2$  time, here  $t_{pd1}$  &  $t_{pd2}$  are the propagation delays of monoshots M1 and M2 respectively.



M1 is triggered with positive going edge of input pulse & M2 is triggered with negative going edge of output pulse of M1

Figure 2: Positive and Negative Edge Triggering

Both adjusted delay and width will be independent of the input pulse width  $t_i$ . The waveforms for input and output pulses are shown in figure 3.

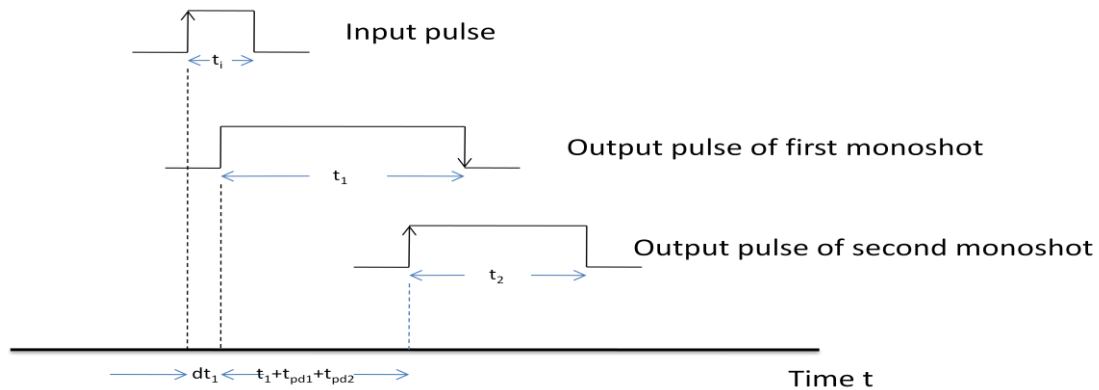


Figure 3: Input and output pulse waveforms

In other methods, delay is adjusted by a digitally programmable delay generator chip which provides programmed delays which can be controlled through n-bit digital word by setting up the bits as shown in Fig. 1 by a parallel block connected by the dotted lines.

### III. Proposed delay generator design (one channel)

The schematic of FPGA based one channel programmable delay generator is represented in Fig. 4, it has following sections, viz. interface control logic, masking register, comparator, for prototype we have used 10 bits (sufficient to achieve the required parameters) for adjusting the required delay and width.

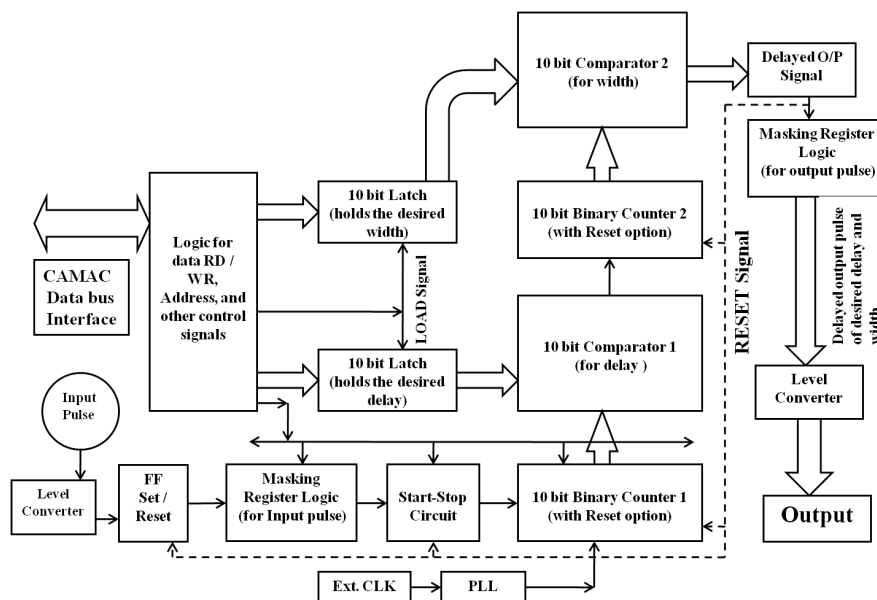


Figure 4: Schematic of single channel of programmable digital delay generator

#### IV. Design of 8 channel programmable delay generator

The module we have proposed is an FPGA based eight channel programmable delay generator with independent delay and width control. It is designed using CAMAC standard for programmability of delay and width adjustment with a 10 bit resolution. We have used Altera Cyclone series (EP1C20F400C8) FPGA. The overall functionality of the 8 channel programmable delay generator is depicted in Fig. 5.

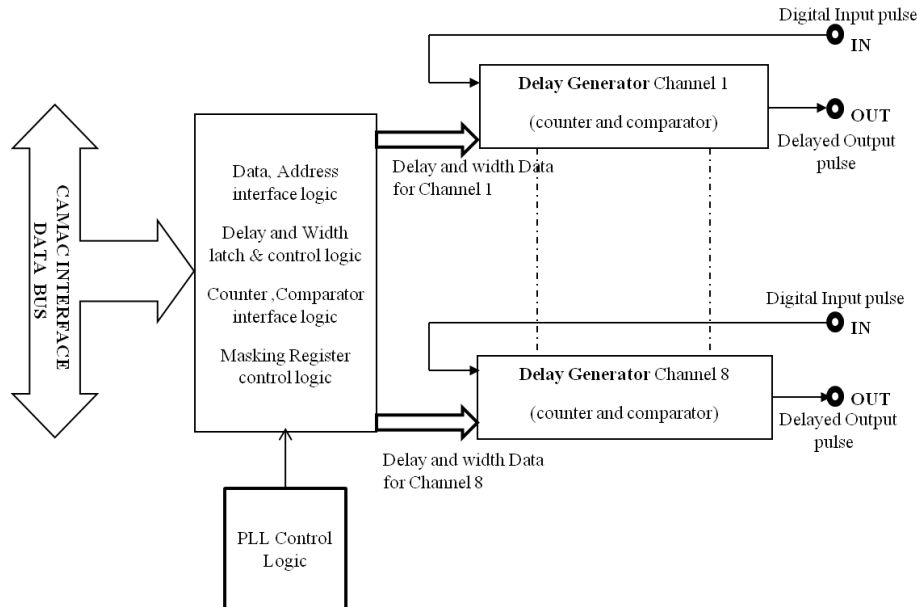


Figure 5: Block diagram of an 8 Channel digital delay generator

The delay and width of each channel are controlled by a 10 bit comparator, and the module is interfaced with CAMAC bus for user programmability of individual channel. The LEMO connectors mounted on the front panel are used for connecting all digital inputs and the corresponding delayed outputs.

#### 4.1 Delay and width control

This section mainly controls the delay and width for individual delay channel over a range which will be decided by the input clock frequency and the number of bits assigned for delay and width respectively. The resolution of the device is limited with the frequency of the input clock. It comprises of mainly four sub-units called CAMAC interface, Latch / Register, counter, and comparator. The CAMAC interface decodes the CAMAC commands issued by user program and loads the delay and width digital word number to the input latches of the addressed channel.

This latched data for each channel are compared, with the output value of two separate counters (one each for delay and width), by two separate comparators of the respective channel and finally desired output waveform is generated. A provision is also made to load the minimum default values for delays as well as for widths for all the channels during the initializing mode and provision is made so that end user can also set the fixed amount of delays and widths for all the channels.

The amount of delay and width is a function of number of bits used and maximum clock frequency used for FPGA.

#### 4.2 Counter Section

In proposed design, we have used two separate counters one each for delay and width for each channel. The first / delay counter (used as delay counter) starts counting input clock pulses as soon as it detects the rising edge of the input digital pulse, while the second counter, which is used for width, starts counting input clock pulses as soon as it detects the rising edge of the output pulse of the first comparator which is used for delay. In our design we have used 500 MHz clock frequency.

#### 4.3 Comparator section

The comparator section has two separate sub comparators, one each for delay and width. These comparators compare the two separate digital word values of delay and width for each channel. The comparator used for delay purpose, starts comparison of the output value of the first counter with the stored delay value in the register used for delay of the respective channel. After the completion of delay comparison, first comparator

gives a high output and then at this point, second comparator starts comparison of the output value of the second counter with the stored width value in a separate register used for width of respective channel.

Finally at the end of this second comparison, a delayed (as desired) output pulse of the required width will be made available at the output of the module for further use.

**4.4 Masking**

In proposed design, we have used the new concept of masking by which we can mask, any particular channel either at the input or at the output side of the module, remotely. In our design, we have used two separate making registers (size of the masking register is as per the required number of channels) for masking input and output channel independently. We have used two 8 bit masking registers each one for input and output masking. Particular channel can be masked by sending a channel number, a control signal for input and output masking register using the CAMAC command word.

In commercial or other home made available delay generators; there is no provision to stop the participation of a particular channel in the process of data recording. In all these available modules, physical presence of end user is necessary to stop the participation of a particular channel by either removing the input or the output cables which are further connected to the front end signal processing setup of the Data Acquisition System.

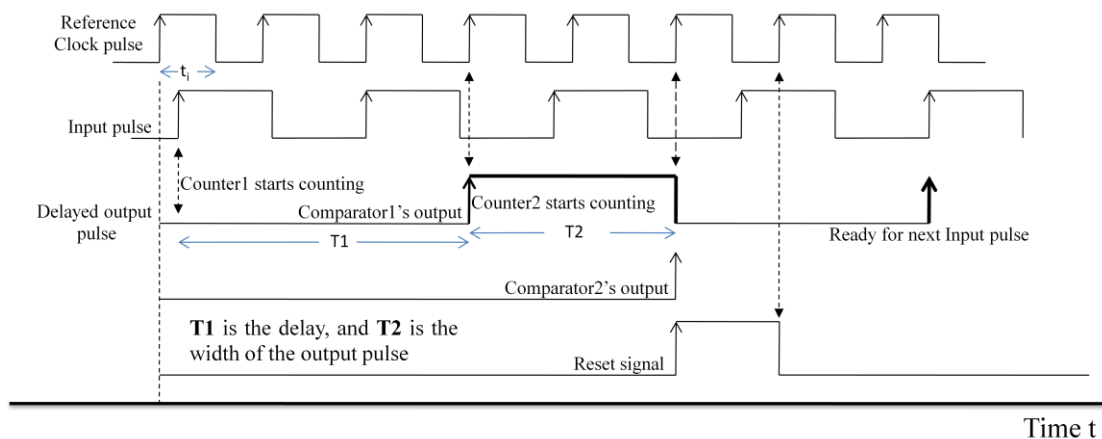
**V. Working**

The rising edge of the input pulse sets a FF1 and then this latched output signal of the FF is used as the enable signal for the first counter1 (used for delay) the counter starts incrementing and output value of the counter are compared in first comparator1 (used for delay) as soon as the output result of the counter1 are equal to the desired value of required delay, the comparator1 gives an output signal1 and at this instant counter1 stops counting.

The rising edge of this output signal1 is the rising edge of the delayed output pulse. The signal1 remains in the high state till the comparison in the comparator2 is not finished.

This output signal1 of the comparator1 enables second counter2 (used for width), the output value of the counter2 are compared in second comparator2 (used for width) as soon as the output result of the counter2 are equal to the desired value of the required width, the comparator2 gives an output signal2 and at this instant counter2 stops counting and at this instant a reset signal of one clock cycle is generated to initialize the counter1, counter2, and FF1.

The rising edge of this output signal2 brings the signal1 in the low state and forms the falling edge of the delayed output pulse, and at this instant the system is again ready to accept next input pulse. Input output waveforms are shown in Fig. 6.



**Figure 6:** Input pulse and delayed output pulse of required delay and width

**5.1 Interfacing**

We have used CAMAC standard data bus for interfacing.

**5.1.1 CAMAC (Computer Automated Measurement And Control)**

CAMAC is an IEEE Std. 488-1978 Bus. A sequence of CAMAC commands are to be written in the user program as per the need of the application.

The format of a typical CAMAC command is N, A, F, 24\_bit Write data or it returns 24\_bit Read data: Where, N is Station address, A is Station sub-address, F is the function.

### 5.1.2 Commands

The valid CAMAC commands for programmable delay generator module are listed below:

- N, F16, A0 to A7, D15....D0 – write /set delay for addressed channel with S1 trailing.
- N, F16, A0 to A7, D19....D16 – write /set width for addressed channel with S1 trailing.
- N, F17, A8 to A15 – Mask addressed channel input – A8=1 is mask; A4, A2, A1, A0 is address with S1.
- N, F17, A0 to A7 – Unmask addressed channel input – A8=0 is unmask; A4, A2, A1, A0 is address with S1.
- N, F18, A8 to A15 – Mask addressed channel output – A8=1 is mask; A4, A2, A1, A0 is address with S1.
- N, F18, A0 to A7 – Unmask addressed channel output – A8=0 is mask; A4, A2, A1, A0 is address with S1.
- N, A(x), F(9), data(x) or C or Z command initializes all Latches to zero value. Where, x denotes don't care.

## VI. Calibrations

We have designed and tested the prototype with the following specifications.

- Delay Range 550ns (max. 2048ns)
- Width 250ns (max. 2048ns)
- Resolution 2ns
- Delay Jitter less than 1ns
- Number of channels 2
- Inputs & Outputs Low Voltage TTL (LVTTTL)

## VII. Simulations

A large number of simulations were done using ModelSim-Altera 10.0c (Quartus II 11.1) Starter Edition. Some of the simulated results, for different combinations of input-output features, are shown in Fig. 7a, and 7b respectively.

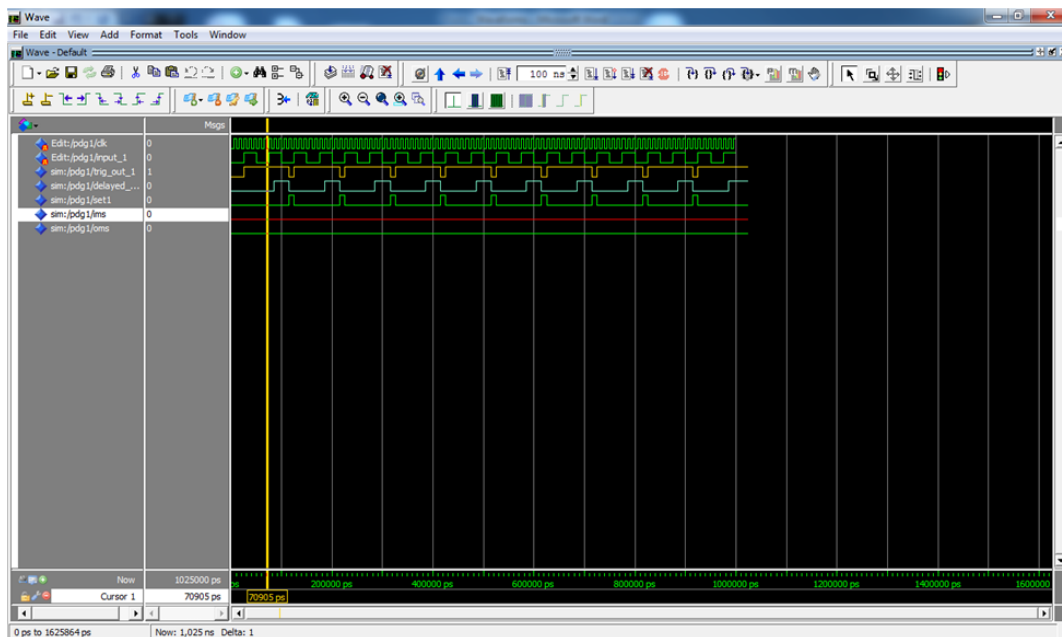


Figure 7a: Input-output pulses for 2 channels without masking

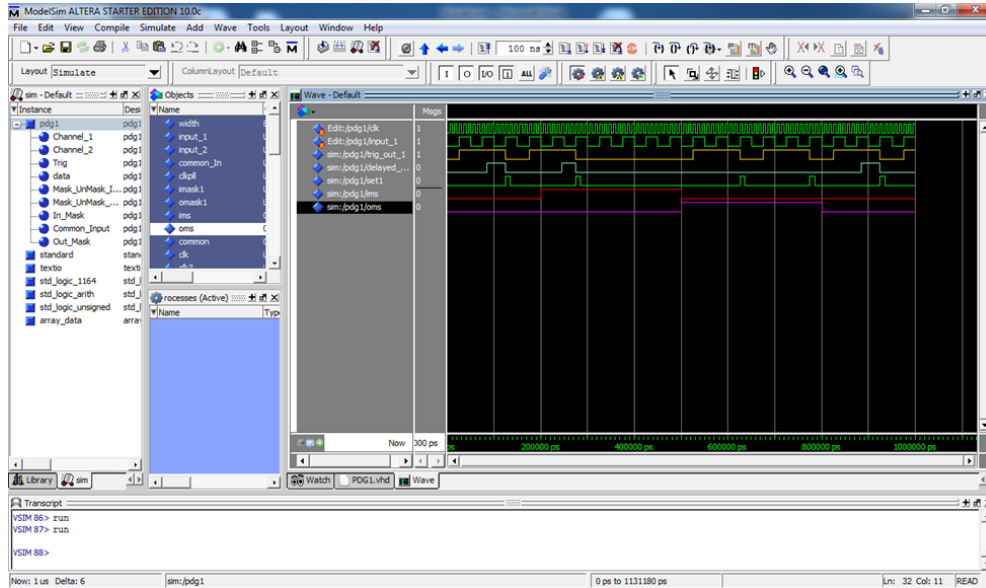


Figure 7b: Input-Output pulses for channel 1 with input and output masking

### VIII. Testing

A large number of tests have been conducted to check the stability of the prototype and it was found that the delays and widths are stable over a period of time, for input signal of different frequencies (low and high ranges) are shown in the Fig. 8a, and Fig. 8b respectively.

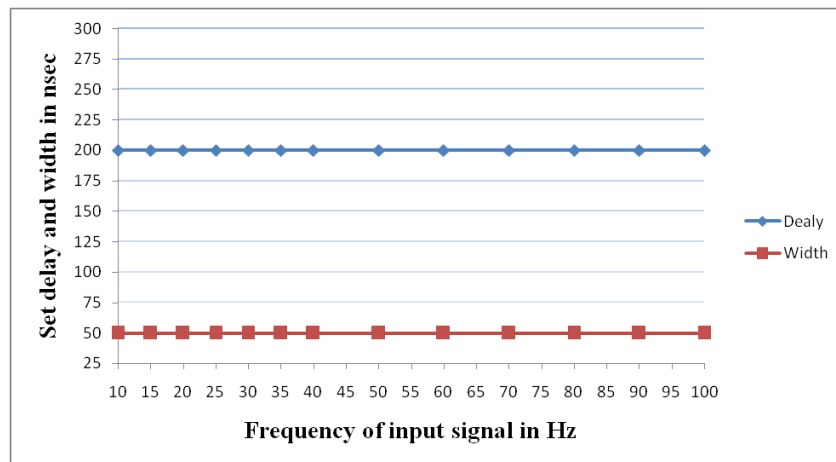


Figure 8a: Stability of delay and width with low frequency range

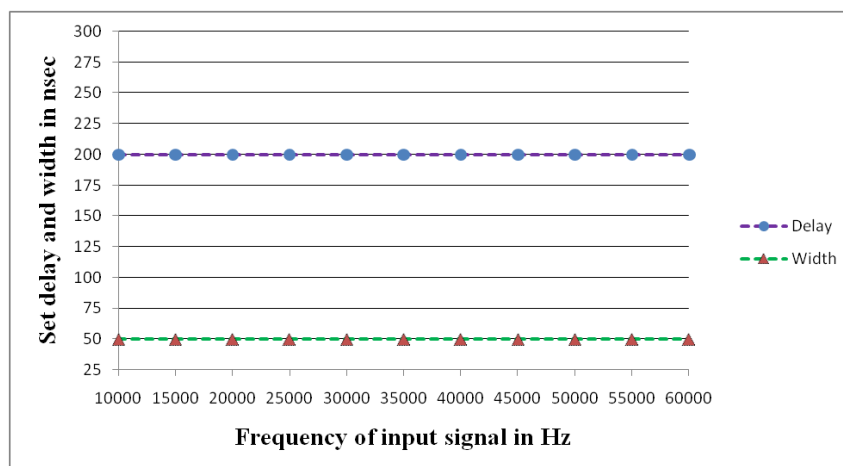


Figure 8b: Stability of delay and width with high frequency range

## IX. Performance

A large number of samples of relative time of outputs of designed delay generator and reference commercial delay generator, and standard length of coaxial cable with respect to a common input reference are recorded using a Lecroy make Time to Digital Converter (TDC)<sup>[8][12]</sup> with a resolution of 250 ps.

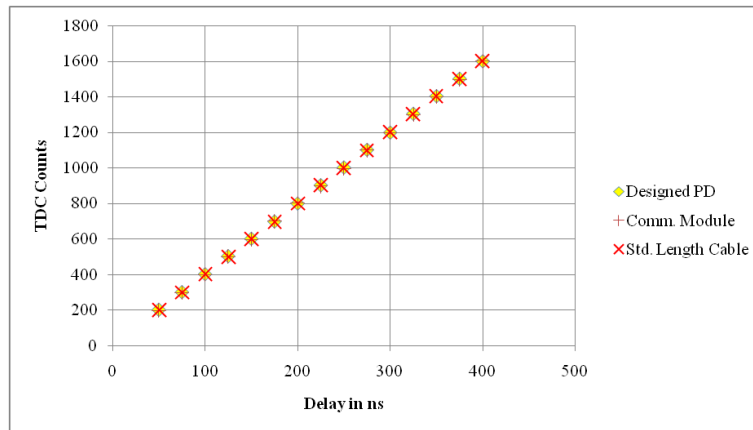


Figure 9: Comparative study

Results of comparative study is shown in Fig. 9 and from the graph it is very clear that designed module is consistent and satisfactory and it is following the same pattern (line) as of commercial module and standard length cable.

## X. Conclusion

Various design features as well as simulations, and actual results of an FPGA-based programmable digital delay generator have been presented here. A prototype of 2 Channel Programmable Delay Generator is fabricated and tested for its functionality. The performance of both the channels of the module is consistent and satisfactory.

The chief advantages of this module are

- The delay & width of individual channels could be set remotely.
- The wider range of delay and width could be achieved.
- Rise time and fall time are well within the limits of 1.5ns.
- Provisions for setting common delay and width in all channels.
- Minimum delay and width at the time of power on.
- Provision for masking any input or output signal independently.
- Stability of delay and width are very good.
- Jitter in delay and width are less than 1ns.
- Easy expandable for more numbers of channels.
- Less power consumption.
- Less propagation delay.
- Low Cost.

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